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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MATTHEW, AARON D	

ART UNIT	PAPER NUMBER
2114	3

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,179	CHEUNG ET AL.	
	Examiner	Art Unit	
	Aaron D Matthew	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Figure 4, element 400. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.
2. Claims 1-17 have been examined.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 6-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

   Claim 6 recites the limitation "said switching the active memory" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim. Examiner suggests including the step of, "switching the active memory from a first memory to a second memory," prior to the mention of said limitation.

Claim 7 recites the limitation "said breakpoint service routine" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim. The language of claim 6 mentions a "breakpoint request," (line 2), but does not disclose a breakpoint service routine. A breakpoint service routine seems to be introduced in claim 8. Examiner suggests either changing the language of claim 6 to introduce the breakpoint service routine, or reordering the claims so as to make claim 7 dependent on claim 8.

Appropriate correction is required.

Claims 8 and 9 are rejected based on their dependence on claim 6.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-15 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Jones et al, (U.S. 6,356,960).

Regarding claims 1 and 17, a method for implementing a breakpoint, (see col. 2, lines 21-24), debugging scheme, (note Abstract), is disclosed, comprising:

- Storing application code in a first memory, (col. 2, lines 16-18);
- Storing a breakpoint service routine in a separate second memory, (col. 2, lines 12-13);
- Encountering a breakpoint request, (col. 10, lines 16-18 and col. 9, lines 25-26);
- Switching the active memory from said first memory to said second memory, (col. 2, lines 10-13); and
- Executing said breakpoint service routine stored in said second memory, (col. 2, lines 12-13).

The debugging routine taught by Jones et al. involves suspending the normal operation of a processor, obtaining a debugging routine from a secondary memory, executing the routine and then resuming the normal operation of the processor. Therefore, a debugging routine as taught by Jones et al. is considered synonymous with a breakpoint service routine as taught by applicant.

As per claim 2, see col. 2, lines 13-18, wherein the active memory is switched from the second memory to the first memory upon completion of the debugging routine.

Regarding claim 3, note col. 2, lines 22-27, which teaches storing status information in a memory stack, ("address store"), prior to switching the active memory from the

first memory to the second memory, and also, reading said status information from the memory stack upon completion of said breakpoint service routine.
To one of ordinary skill in the art, the use of a memory stack is inherently taught by Jones et al in the language, "address store."

As per claim 5, when a suspend operation is in effect, the operation of the CPU in accessing the first memory is inhibited, (see col. 12, lines 12-18). Since the second memory is only active during a suspend operation, (note col. 2, lines 6-18), thus enabling the debugging routine, it is inherent in this disclosure that the first memory is not accessible when the second memory is active.

Regarding claim 4, and in view of the above explanation pertaining to claim 5, with the first memory only being active in the absence of a suspend state, it is also inherent that the second memory is not accessible when the first memory is active. The second memory is only accessible during a suspend operation.

Regarding claim 6, and as applied to claims 1 and 17 above, Jones et al discloses a method for implementing a memory scheme comprising:

- Receiving a breakpoint request, (col. 2, lines 9-12; col. 10, lines 16-18; and col. 9, lines 25-26);
- Storing status information in a memory stack prior to said switching the active memory from a first memory to a second memory, (col. 2, lines 22-27);

- Changing memory references from said first memory to said second memory, (col. 2, lines 10-13); and
- Operating a program stored in said second memory, (col. 2, lines12-13).

The use of memory references is inherent in the operation of multiple memory devices, as would be obvious to one of ordinary skill in the art when viewing the language of col. 2, lines 10-13. Note also, col. 1, lines 66-67.

As per claim 7, it is inherent that in operating the CPU with code in said first memory after the completion of said debugging routine, (note col. 2, lines 16-18), the memory reference would be restored from said second memory to said first memory. Note also, col. 2, lines 22-27, which teaches reading the status information from a memory stack upon completion of the debugging routine.

Regarding claim 8, note col. 2, lines 12-13.

As per claim 9, see col. 2, lines 13-18.

Regarding claim 10, a system for non-intrusive dynamic memory mapping, (note col. 14, lines 49-54), is disclosed, comprising:

- A processor, (col. 1, line 35);
- A first memory for storage of application code, (col. 1, lines 49-51);

- A second memory for storage of a breakpoint service routine, (col. 1, lines 45-46), said second memory configured separate from said first memory, (col. 1, lines 50-51); and
- A controller configured to select one of said first memory and said second memory, (col. 1, lines 43-46), based on the status of said processor, (col. 8, lines 41-46).

Also, see col. 1, lines 37-38 which discloses a communication path between the CPU and the first memory, and col. 1, lines 39-41, which discloses a connection between said controller, second memory, and said communication path. This system, therefore, inherently discloses a controller coupled between a processor, a first memory and a second memory.

As per claim 11, note, again, col. 10, lines 16-18, and col. 8, lines 41-46, wherein the state of said processor includes information regarding the breakpoint, or suspension, status of said processor.

Regarding claim 12, note col. 1, lines 35-37, which teaches a bus interface coupled to said first memory, said second memory, said processor, and said controller. See explanation regarding the communication path, as pertained to claim 10 above.

Regarding claim 13, said bus interface is configured to send and receive data to and from said first memory, (col. 1, lines 37-38), and said second memory, (lines 40-42),

and further configured to send and receive data to and from said processor, (lines 37-38), based on instruction received from said controller, (lines 42-43).

As per claim 14, the bus interface is configured to access only one of said first memory and said second memory based on signals provided by said controller. This behavior is inherent in the design taught in col. 1, lines 42-50, but is further detailed in the explanation of the suspend logic given in col. 12, lines 12-18.

Regarding claim 15, see col. 1, lines 42-46, wherein said controller is configured to select said second memory when a breakpoint interrupt service request is made.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. as applied to claim 10 above, and further in view of Kamiya, (U.S. 4,672,534).

Jones et al. fails to disclose a second memory that is a read-only memory.

Kamiya teaches a second memory that is a read-only memory and stores a test program, (see col. 1, lines 50-52).

Kamiya and Jones are considered to be analogous art because they both teach a system for storing a debugging routine in a secondary memory, to be accessed separately from a first memory in response to a debugging control unit.

The second memory as disclosed in the preferred embodiment of Jones et al. is accessed only in order to read a debugging routine stored therein. In this embodiment, the capability to write to the second memory is not required, and therefore a ROM device would be sufficient in performing the functions of the second memory, and would further offer the advantage of preventing the debugging routine stored therein from being altered. In view of Kamiya one of ordinary skill in the art would have found it obvious to include a ROM device as a second memory in Jones et al, and would have been properly motivated to do so in order to protect the integrity of the debugging routine stored in the second memory.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double

patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 10-15 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 13 of copending Application No. 10/128,025. Although the conflicting claims are not identical, they are not patentably distinct from each other.

It is well settled that the omission of an element and its function is an obvious expedient if the remaining elements perform the same function as before. In re Karlson, 136 USPQ 184 (CCPA 1963).

Claims 10-15 omit the following elements from copending Application claim 13: a breakpoint interrupt generator configured to transmit signals when a breakpoint is desired. Claims 10-11 and 15 further omit a bus interface coupled to a microcontroller and to a dynamic memory mapping controller.

Regarding claim 10, claim 13 of the copending application comprises the following:

- A system for non-intrusive dynamic memory mapping *, (line 5);
- A processor, (lines 1-2);
- A first memory, storing application, (program), code, (line 11);

- A second memory, storing a breakpoint service routine **, configured separately from the first memory ***, (lines 10-11);
- A bus interface coupled to said microcontroller and to said dynamic memory mapping controller, (lines 8-9), and coupled to the breakpoint memory and the program memory, (lines 10-11). Thus, inherently, the system comprises a controller coupled between a processor, a first memory and a second memory.

*A dynamic memory mapping scheme that includes a program memory and a breakpoint memory in separate devices is inherently non-intrusive.

**A breakpoint memory, as described on line 10, implies a memory device storing a breakpoint service routine.

***The separate mention of two distinct memory devices implies their separate configuration.

The language of claim 13 of the copending application states on lines 12-14 that the bus interface is configured to select between said program memory and said breakpoint memory based on a signal from said breakpoint interrupt generator. The bus interface is only coupled to said breakpoint interrupt generator due to the coupling between the dynamic memory mapping controller and the breakpoint interrupt generator, (see lines 5-9. Therefore, it is inherent that the system comprises a controller that is configured to select one of said first memory and said second memory based on the status of said processor, if the bus interface is configured to do the same.

Regarding claim 11, the language on line 14 states that the status of the processor is coming from a breakpoint interrupt generator, which transmits a signal when a breakpoint is desired, (see lines 3-4). Therefore, it is implied that the information pertaining to the status of the processor includes information regarding the breakpoint status of said processor.

Regarding claim 12, the bus interface introduced in lines 8-9 is coupled to the first memory, (line 11), the second memory, (line 10), the processor, (line 8), and to the controller, (line 9).

Regarding claim 13, in being coupled as described above, it is inherent in a bus interface's design, as widely known in the art, that it would be configured to send and receive data to and from the first memory and the second memory, and would also be configured to send and receive data to and from the processor based on instructions received from the controller. Such functionality is inherent in the usage of a bus interface.

Regarding claim 14, it is implied in the language, "select between," as it appears on lines 12-13, "said bus interface is configured to select between said program memory and said breakpoint memory," that only one of said first and second memories is to be accessed. Moreover, as the bus interface is coupled to the

dynamic memory mapping controller, (lines 8-9), it is implied that the signals that determine which memory is to be accessed, originate at the dynamic memory mapping controller.

Regarding claim 15, it is also implied that the second memory, or breakpoint memory, is to be accessed when a breakpoint interrupt service request is made.

Conclusion

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron D Matthew whose telephone number is (703) 605-1211. The examiner can normally be reached on 8:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ADM

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